Device innovation – a bottom-up approach for sustainable growth?

Jörg-Peter Elbers, SVP Advanced Technology

2nd Visions for Future Communications Summit, Nov 27th-28th, 2019, Lisbon

Smart networks - Bringing ICT together

zero-touch operation

instantaneous response

access anywhere

intrinsic security

sustainable capacity growth

From successes in the past …

~1977-92
Regenerated direct-detection systems

~1970
low-loss fiber, semiconductor laser @ room temperature

~1993-2009
Optically amplified, dispersion managed WDM systems

~1990
Erbium-doped fiber amplifier (EDFA)

~2010- ?
DSP-based coherent WDM systems

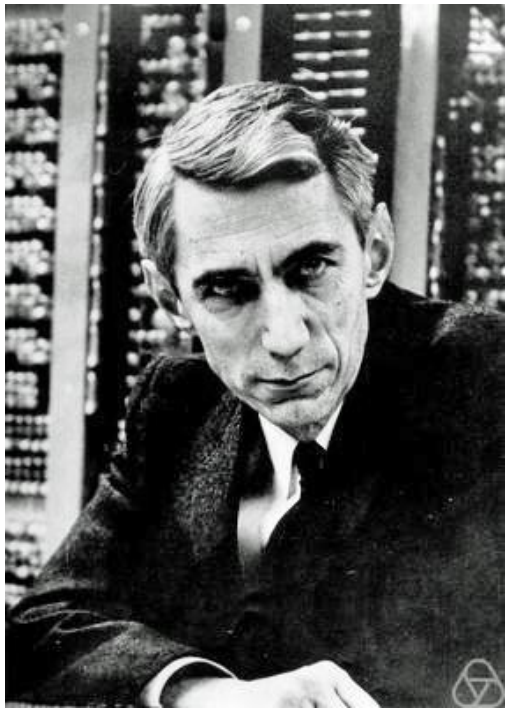
~2010
>50GS/s, >50M gate DSP ASICs

Example: Fiber-optic communications

Component innovation as key enabler for system & network technology

… to challenges of the future

Shannon limit



Claude Shannon by Konrad Jacobs, CC BY-SA 2.0 de

Polarization
Spatial paths
Bandwidth

$$C = 2 \times M \times B \times \log_2 (1 + SNR)$$

Signal-to-noise ratio

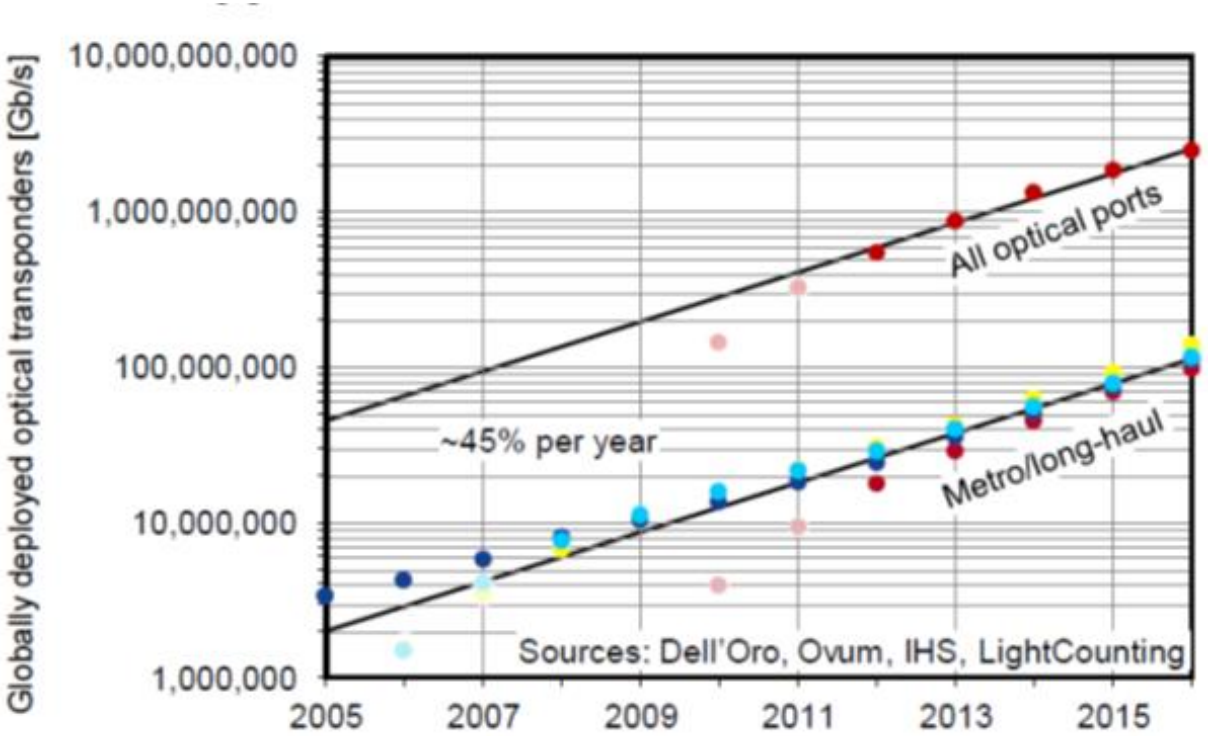
Moore's law

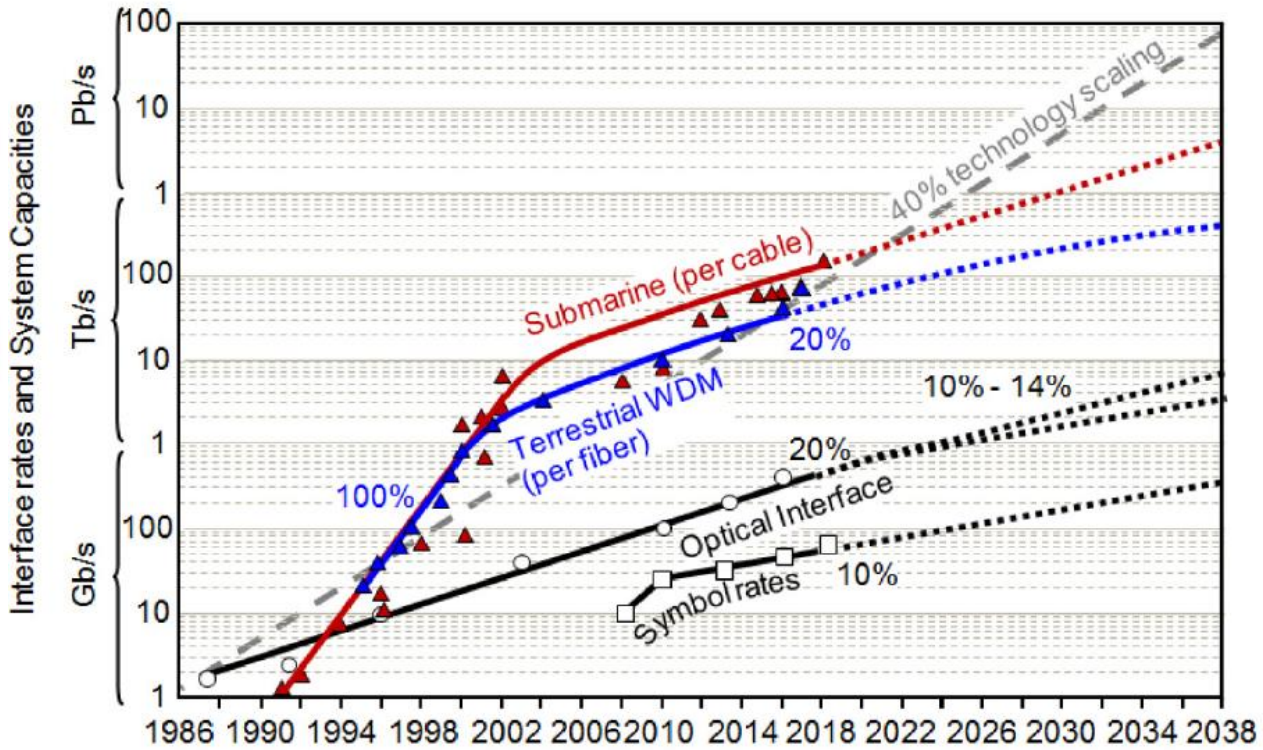
Gordon Moore and Robert Noyce, Intel Free Press, CC BY-SA 2.0

The number of transistors in a dense integrated circuit doubles about every two years.

How far can we push the Shannon limit and Moore's law?

Entering an era of scaling disparities, …

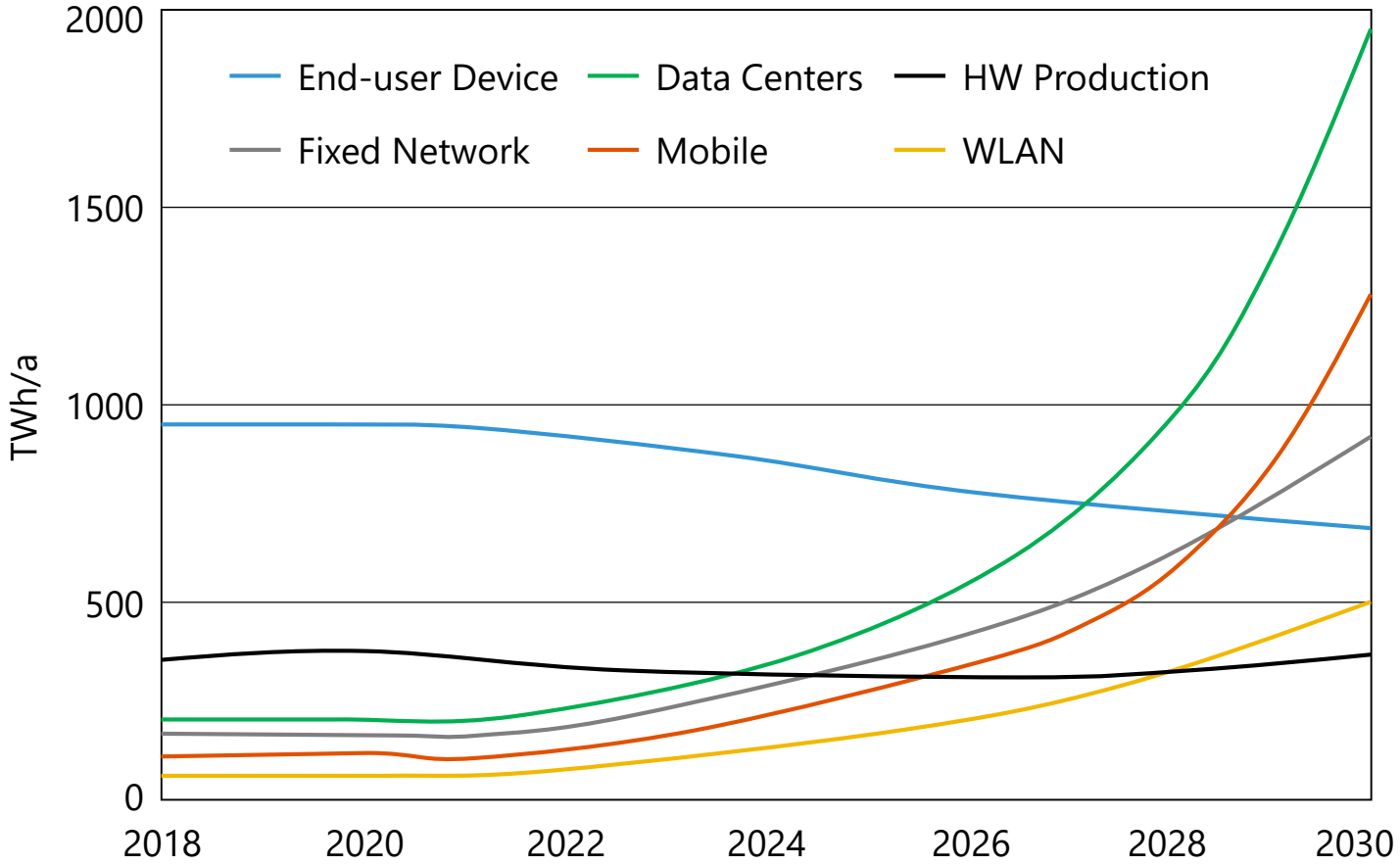




[Source: Peter Winzer et al., Optics Express, Vol. 26, No. 18, Sept. 2018]

How to scale capacity while lowering cost per bit/s/km at the same time?

… energy consumption challenges,



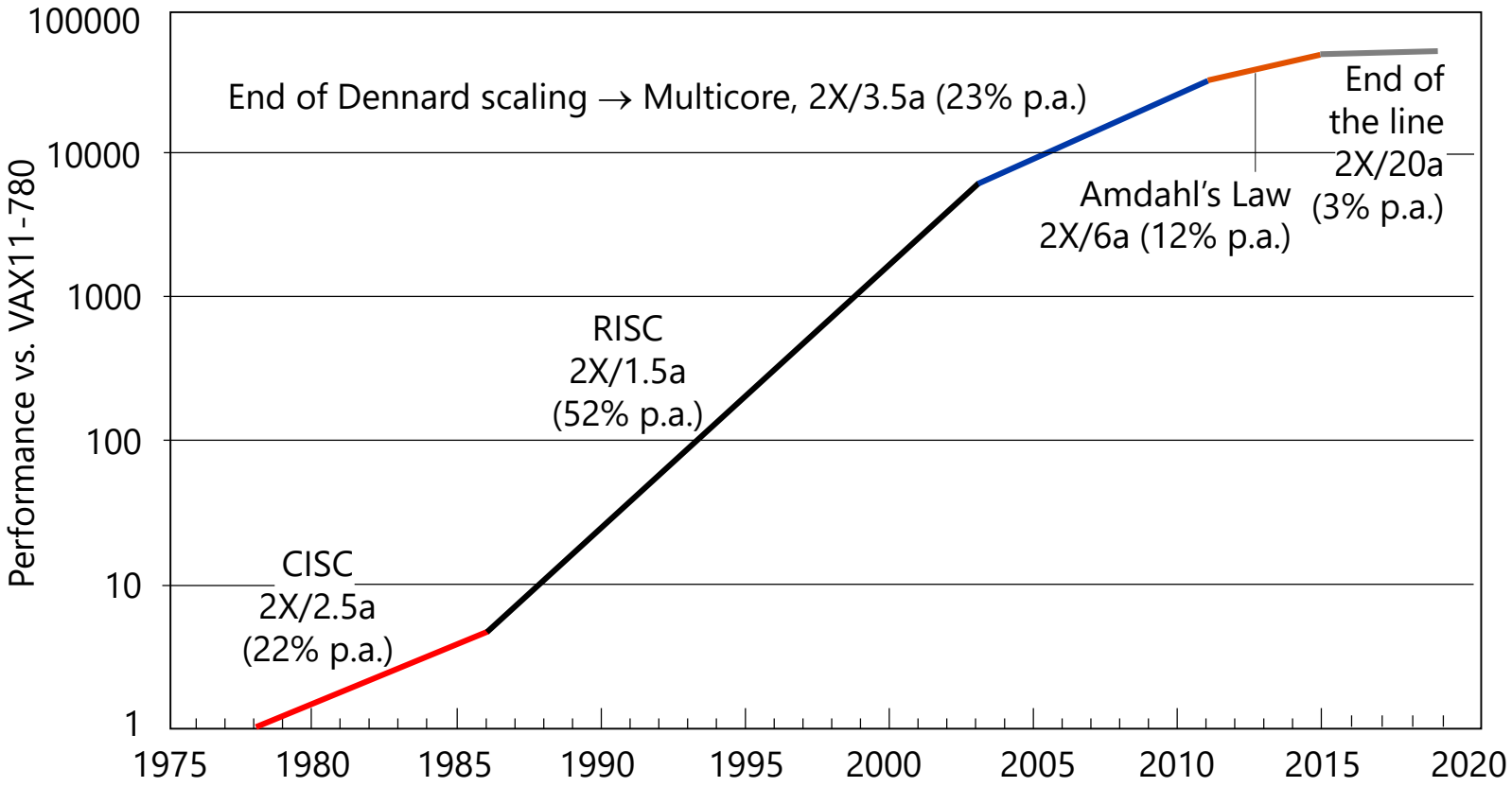
Source: Heise Technology Review 7/2019
Data: A. Andrae, DOI: 10.13140/RG.2.2.25103.02724

"Management is doing things right; leadership is doing the right things."

Peter Drucker

We need to drive more efficiency AND new approaches

… and diminishing CPU performance gains



Source: J. L. Hennessy, D. A. Patterson, Communications of the ACM, 2019, Vol. 62, No. 2

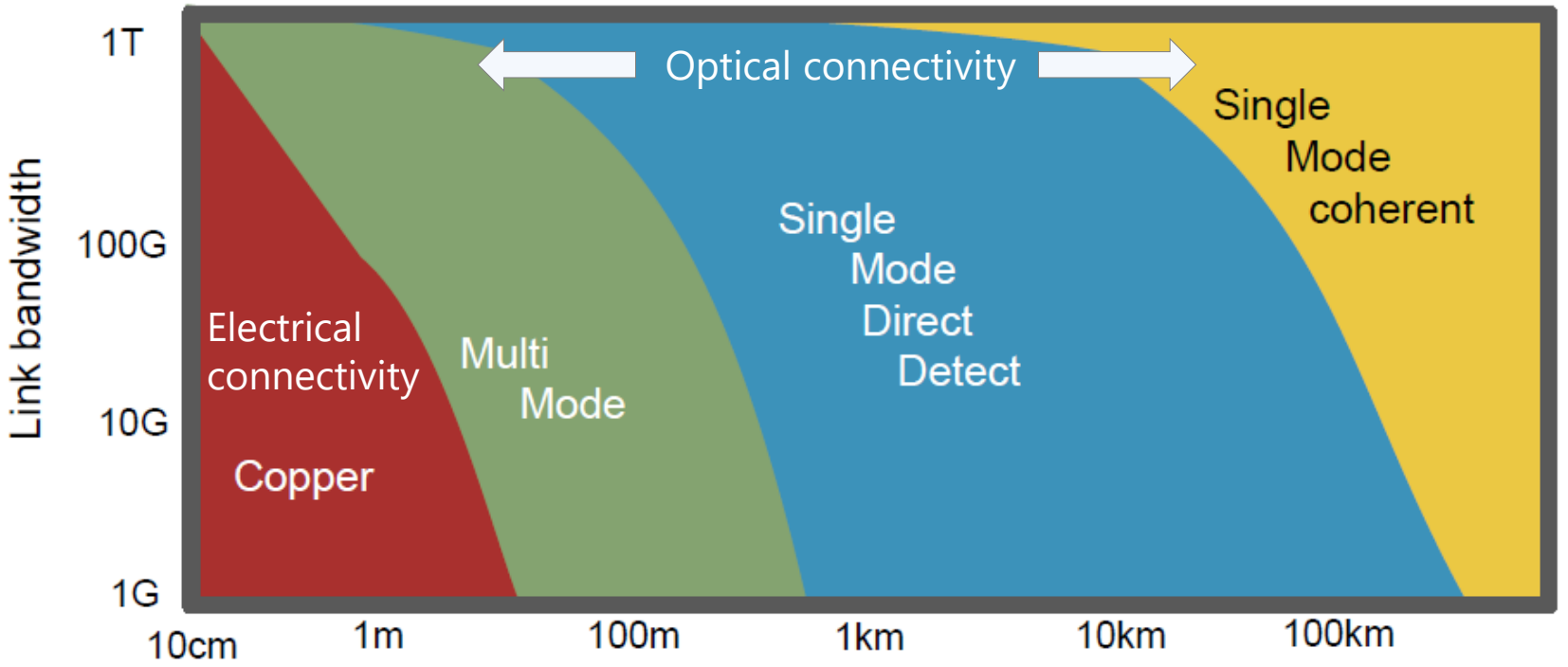
Diminishing returns from parallelism

General purpose CPU architecture not optimized for data-heavy tasks

CISC: Complex instruction set computer
RISC: Reduced instruction set computer
GPU: Graphics processing unit
TPU: Tensor flow processing unit
FPGA: Field programmable gate array

Trend to domain-specific architectures (GPUs, TPUs, FPGA accelerators, …)

Communication demands increase



Source: Finisar

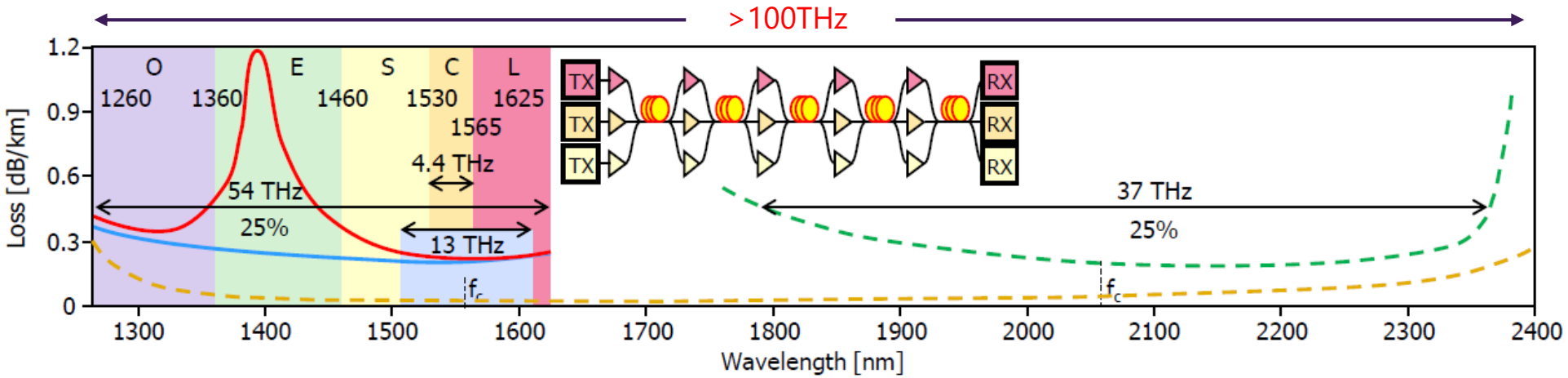
"In parallel processing, 1Mbps of I/O is required for every 1MHz of computation."

Amdahl's lesser known law

High-bandwidth and low power connectivity is needed

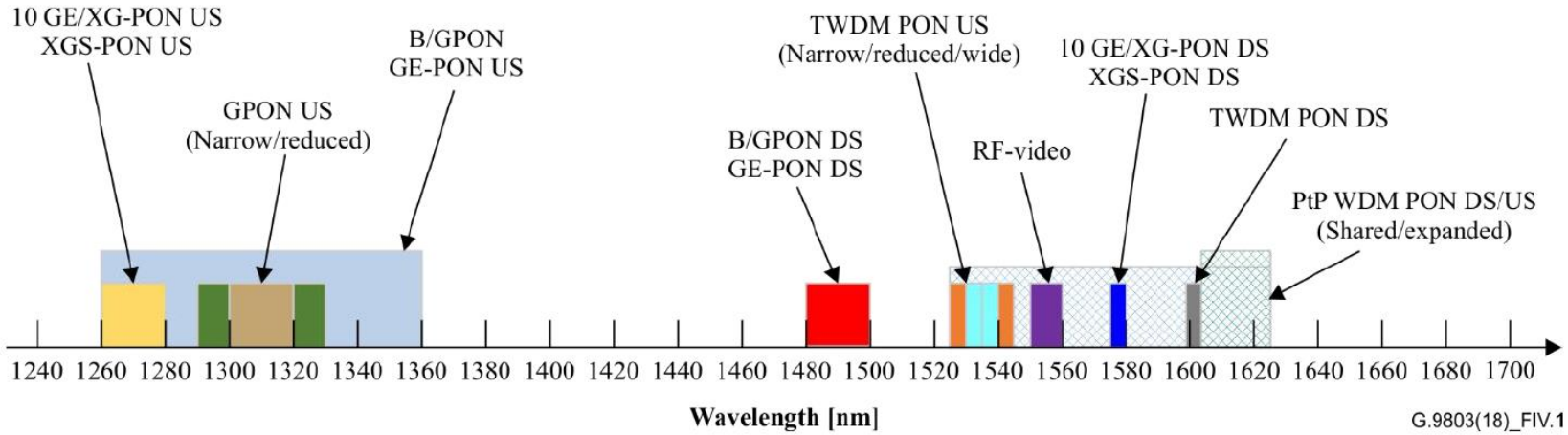
Research & innovation areas

New device developments for all network domains



[Source: Peter Winzer et al., Optics Express, Vol. 26, No. 18, Sept. 2018]

Optical metro & core networks



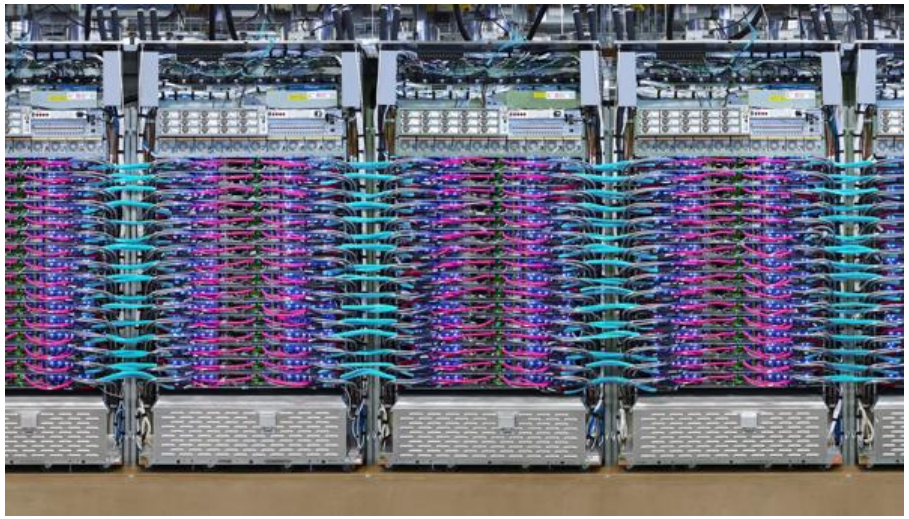
[Source: ITU-T]

Optical access networks

Different network requirements and cost points demand different solutions

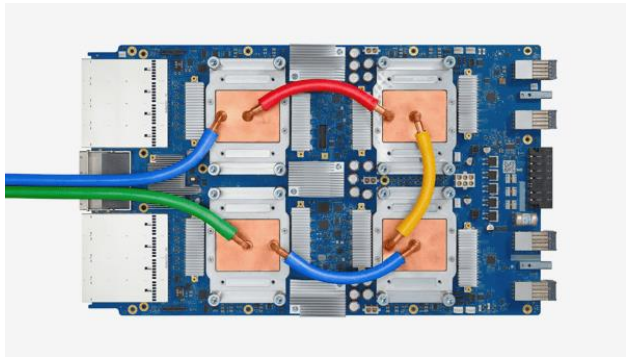
Domain-specific compute architectures

Cloud TPU v3 Pod (Beta):
100 PetaFLOPS, 32 TB HBM, 2D mesh network (ring)



TPU: Tensor Flow Processing Unit
HBM: High Bandwidth Memory

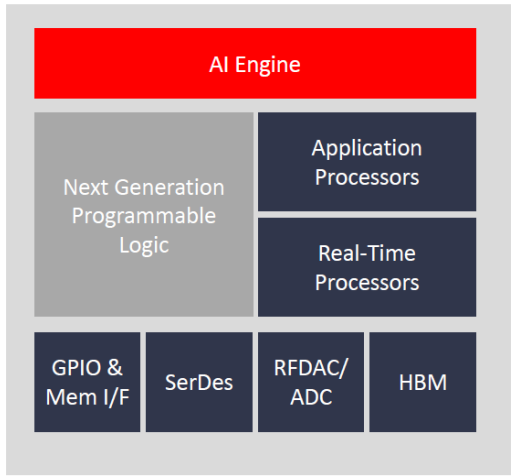
Cloud TPU v3



Source: Google

Google Edge TPU

Adaptive Compute Acceleration Platform



Source: Xilinx

First FPGA Introduced

1985

First Virtex FPGA

1998

Virtex-2 Pro

2001

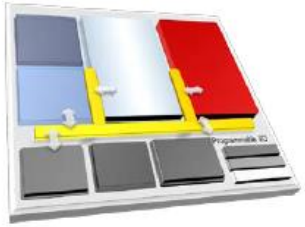
First 3D FPGA & HW/SW Programmable SoC

2011

First MPSoC & RFSoC

2016 / 2017

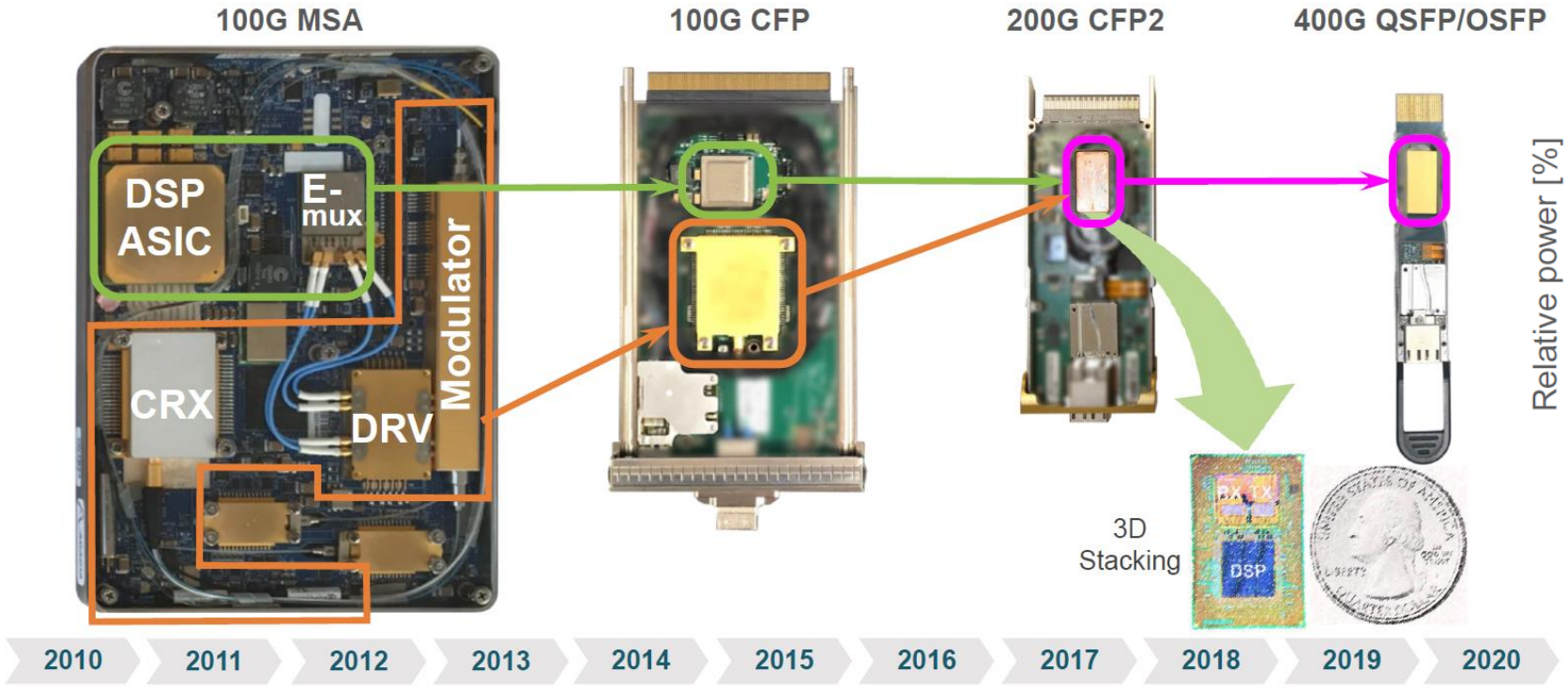
ACAP

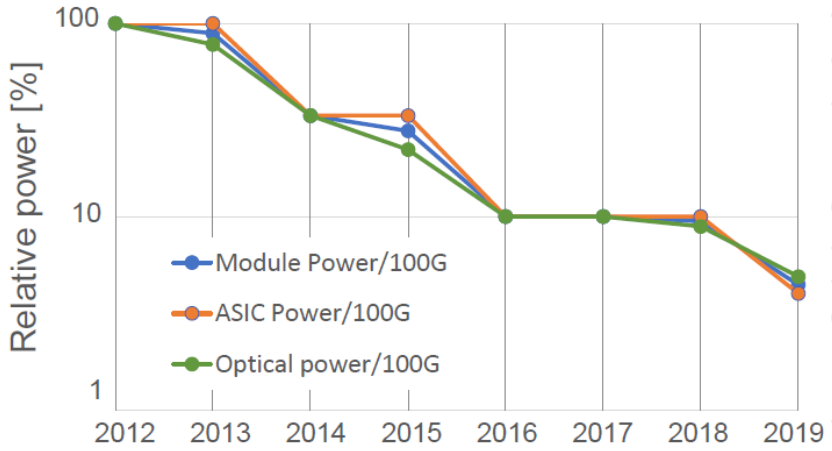


2019

SoC: System on Chip
MPSoC: Multi-Processor System on Chip
RFSoC: Radio Frequency System in Chip
GPIO: General Purpose I/O

Optical & electronic integration

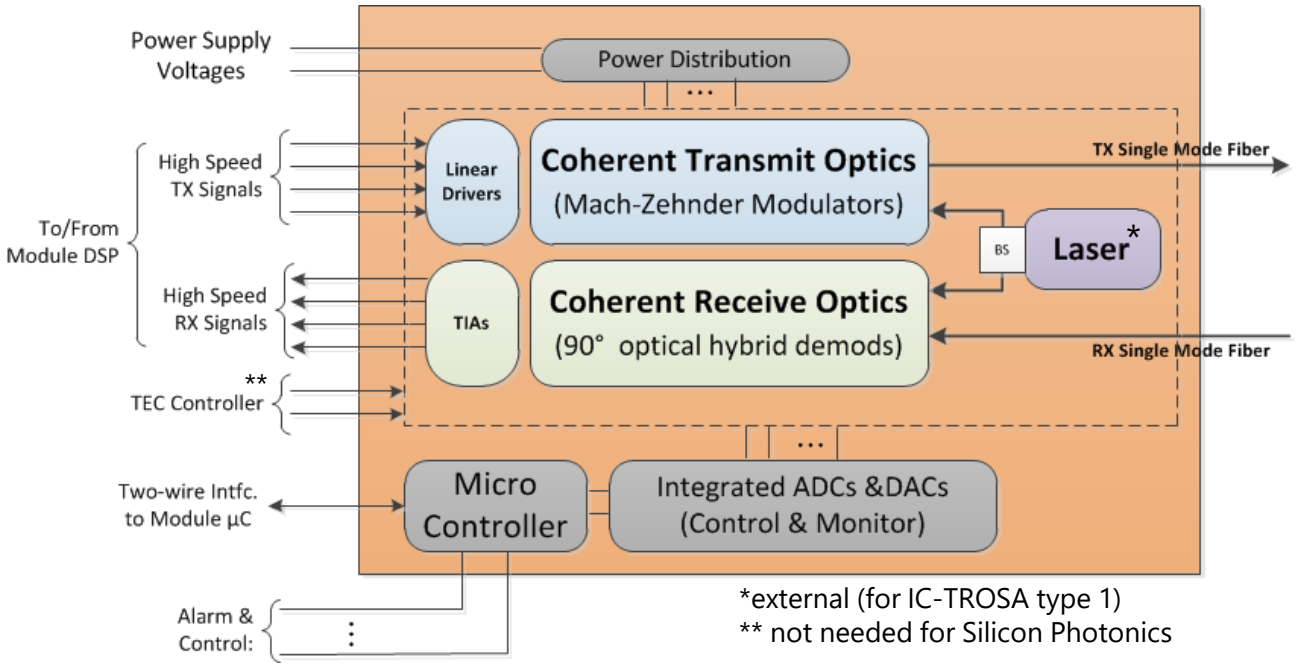




Source: Acacia Communications, 2019

Lower footprint, lower power, lower cost per bit

Integrated coherent TX-RX optical subassembly



*external (for IC-TROSA type 1)
** not needed for Silicon Photonics

TIA: Transimpedance amplifier
TEC: Thermoelectric cooler

IC-TROSA type 1 SMT package
(BGA, reflow-soldering capable)

Electro-photonic integration 2.0

Silicon as base platform

Integration of new materials

InP quantum-dot based laser/amp integration

DIMENSION-

moicana

PEARLS

SPEED

DSP co-integration

Electro-photonic integrated circuit on Silicon:
Coherent Modulator+Driver+Receiver

Pluggable interfaces

ihp

ePIC process
(SiGe BiCMOS & Silicon Photonics)

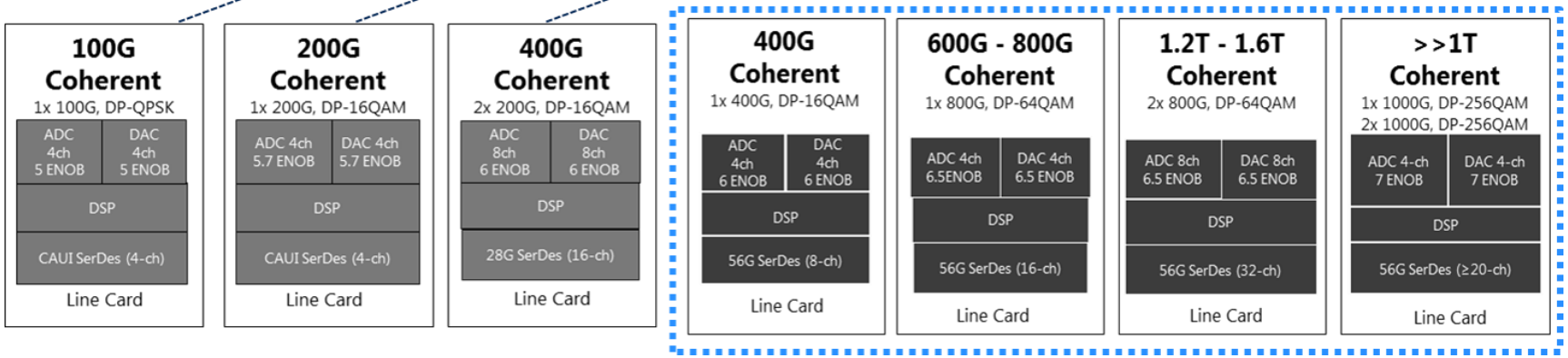
Non-hermetic, uncooled optical transceiver chiplets

ADVA

Coherent optical DSP ASIC advances

|Year	2010	2012	2014	2016-17	2018-19	2020-21
			ADC / DAC PARAMETERS	Next Generations		
POWER (MAX)	<2W/channel	<1.5W/channel	~1W/channel	<1W/channel	<<1W/channel	TBC
RESOLUTION	8-bit	8-bit	8-bit	6-8-bit	6-10 bit	6-10 bit
CONVERSION RATE	56GSa/s	55-65GSa/s	55-92GSa/s	34-128GSa/s	34 to >140GSa/s	34 to >160GSa/s
ENOB	5.5	>5.7	>6	5.5 to 6.5	5.5 to > 8.5	5.5 to >8.5
BANDWIDTH (-3dB)	>16GHz	>19GHz	>26GHz	>35GHz	>42GHz	>49GHz
			ASIC RELATED			
TECHNOLOGY*	65nm CMOS	40nm CMOS	28nm CMOS	16nm FinFET	7nm FinFET	5nm FinFET
DIGITAL GATES (DSP)	>50M	>70M	>200M	>400M	>1000M	>1500M
ADDED FEATURES	-	-	1/2 & 1/4 rate, ASV	1/2 & 1/4 rate, ASV	1/2 & 1/4 rate, ASV, others	1/2 & 1/4 rate, ASV, others
PACKAGE SIZE	35x35mm	37.5x37.5mm	37.5x37.5m	25x25mm	≤25x25mm	≤25x25mm
COHERENT APPL.	100Gbps	200Gbps	400Gbps	400Gbps ≤1Tbps	≤2Tbps	≥2Tbps

ASV: Adaptive Source Voltage



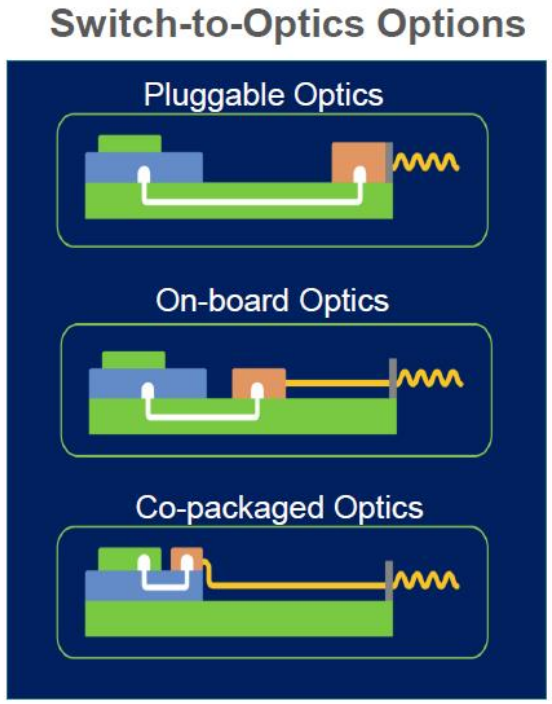
Source: Socionext, 2019

Leading edge CMOS technology

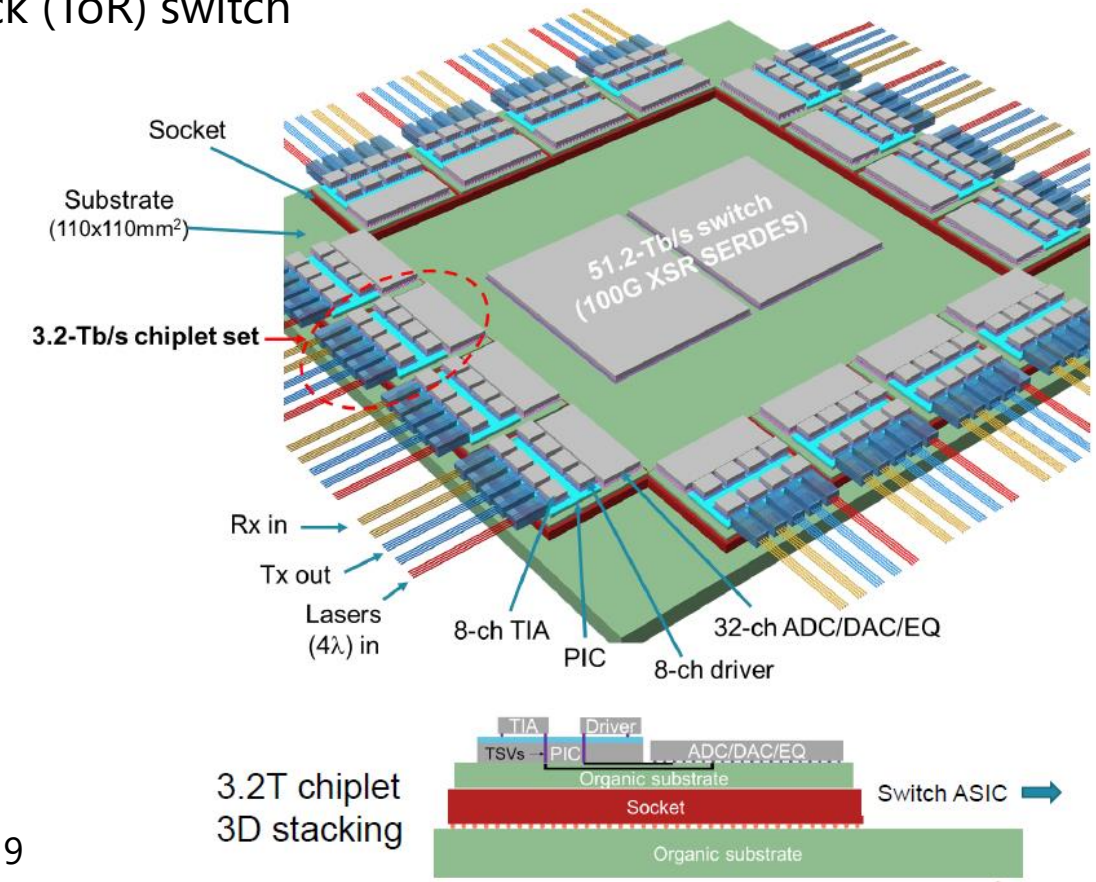
Leverage for future radio modems?

Optical transceiver chiplet integration

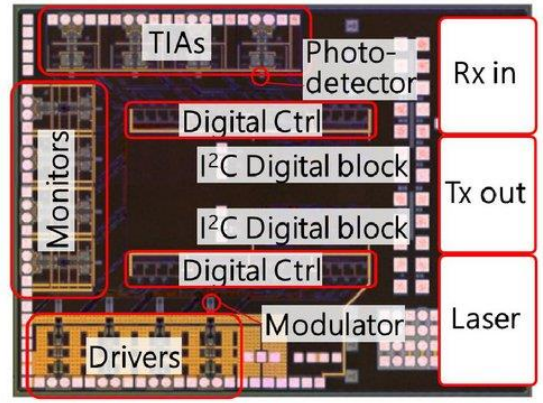
Next generation Top-of-Rack (ToR) switch



Source: Acacia Communications, 2019



100G intra-office transceiver
Monolithic ePIC chiplet



Source: Sicoya, 2016

See also:
https://www.facebook.com/CoPackagedOptics Collaboration

Co-packaging optics with switch, routing, or processing dies

Main take-aways

Sustainable network capacity growth imposes huge scaling challenges

Network, system, and component research need to go hand-in-hand to solve these

Optical connectivity will play an increasing role

Domain-specific architectures and (the right level of) integration are key

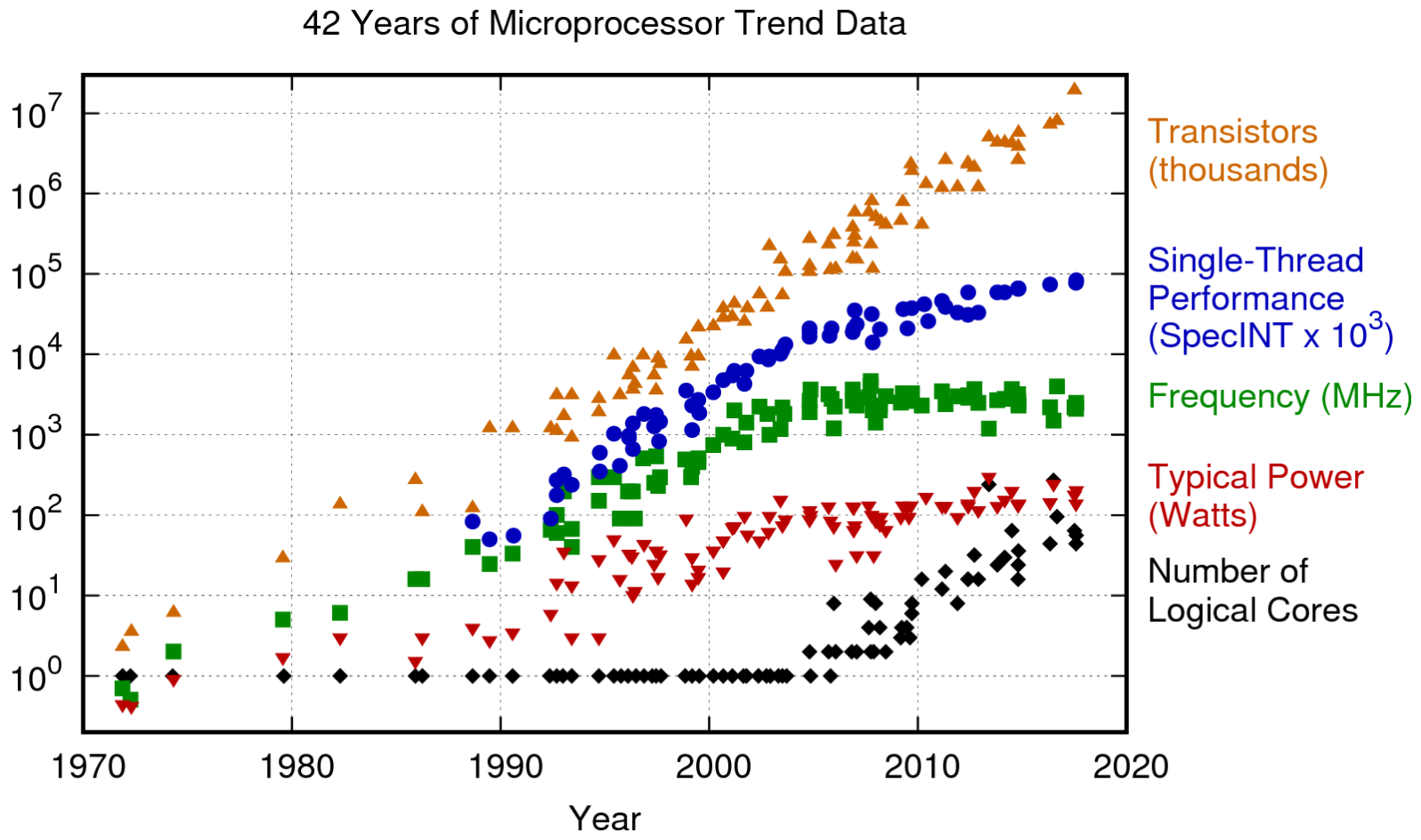
Device-related research and innovation areas (architecture & design, hardware, software):

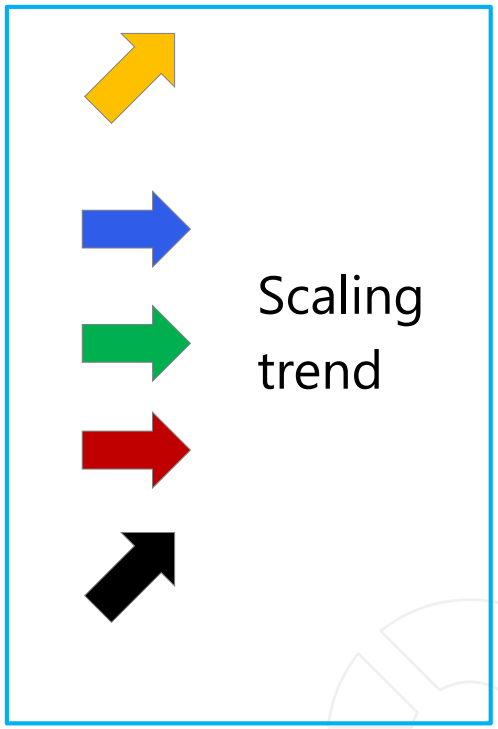
- *Novel System-in-Package/System-on-Chip approaches (multiple technologies, heterogeneous integration, new materials)*
- *Advanced (optical) transceiver chiplets and related digital signal processors*
- *New optical fibers, amplifiers, switching nodes, terminal nodes*
- *Optical-wireless integration (analog/digital) towards "optical radios"*
- *New computing nodes for edge applications (AI inference, video pre-processing, …)*
- *HW-based security functions*

Thank you

jelbers@advaoptical.com

Microprocessor scaling continues …





Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2017 by K. Rupp
https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/

Most recent advances by increasing the number of cores

From chip to chiplet integration

PC-CENTRIC

TRANSISTOR SCALING & MONOLITHIC INTEGRATION

One process design point for all products
Monolithic integration
Product restricted by reticle

DATA-CENTRIC

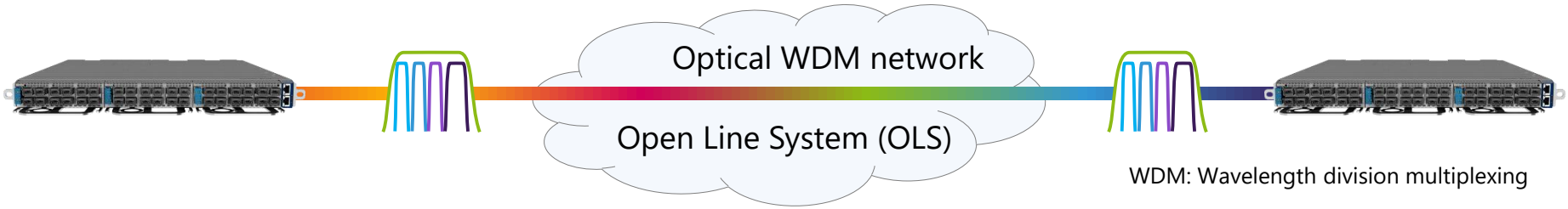
HETEROGENEOUS PROCESSES & INTEGRATION

Multiple processes optimized for individual IPs
Multi-chip integration with advanced packaging
Product unconstrained by reticle

Source: Intel, 2019

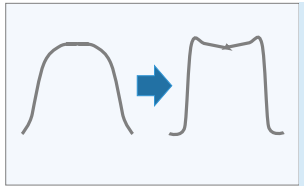
Systems in a package (SiP) comprising different building blocks

Deep-dive: Flexible coherent optics

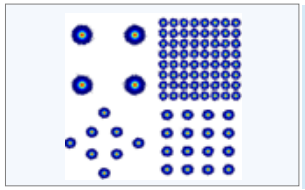


WDM: Wavelength division multiplexing

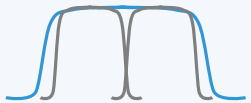
Channel rate - flexible wavelengths



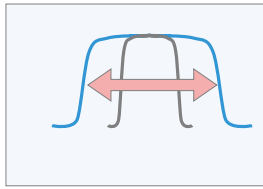
Shaping - channel adaption



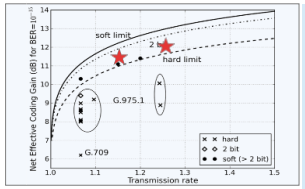
Modulation - with fractional QAM



Channel capacity - multiple lambdas



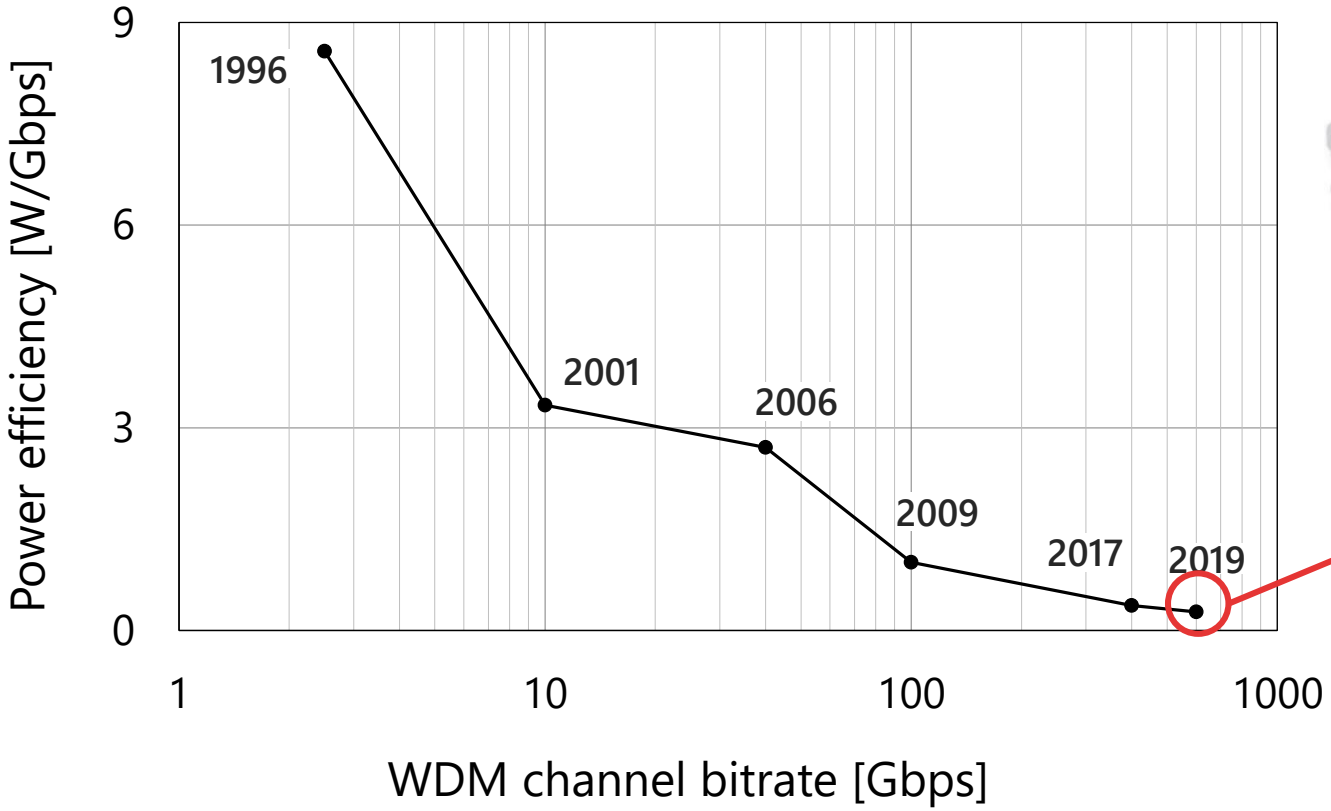
Modulation speed – tunable Baud rate



FEC- ultimate gain and options

The gold standard in WDM networks at 100Gbps and beyond

WDM transport platform evolution



FSP 3000 TeraFlex™

3.6 Tb/s capacity

<0.25 W/Gbps

Eco Design

Increasing capacity while lowering the energy per bit