imec

DEVICES and more…

André Bourdoux

2nd Vision for Future Communications Systems

27 - 28 November 2019, University Institute of Lisbon (ISCTE-IUL)

Technologies for Communications above 100GHz

B5G/6G high capacity applications

Towards Terabit-Per-second wireless connectivity

Close proximity applications

Kiosk, automotive data, D2D

Multi-user AR/VR and holographic display

Fixed wireless Access

Wireless Backhaul/Fronthaul

Fixed point-to-point links for cellular networks

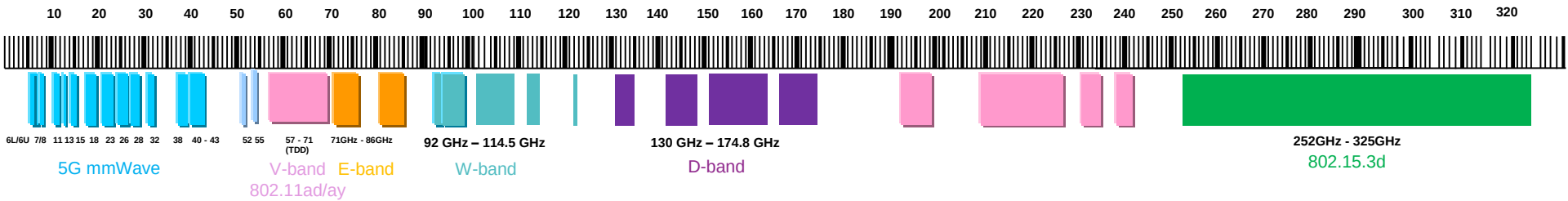
1m — 10m — 100m — >100m

imec

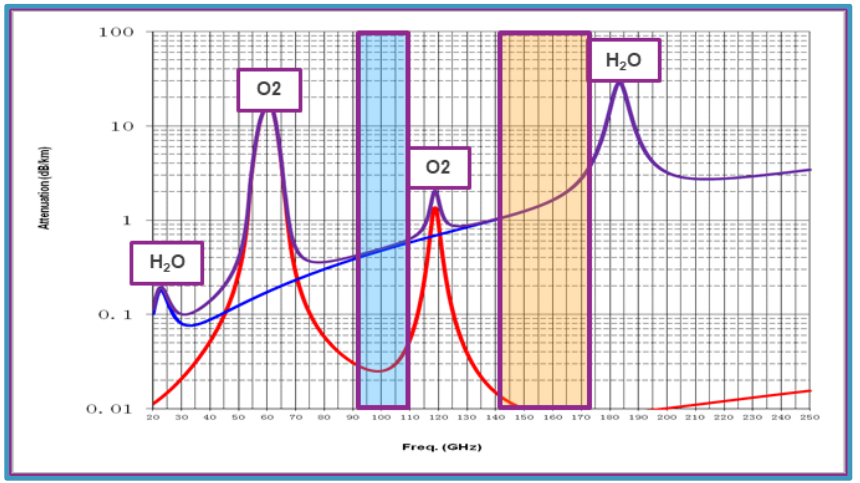
New radio spectrum to meet the 6G capacity Demand

Towards THz frequencies for Tbps wireless connectivity

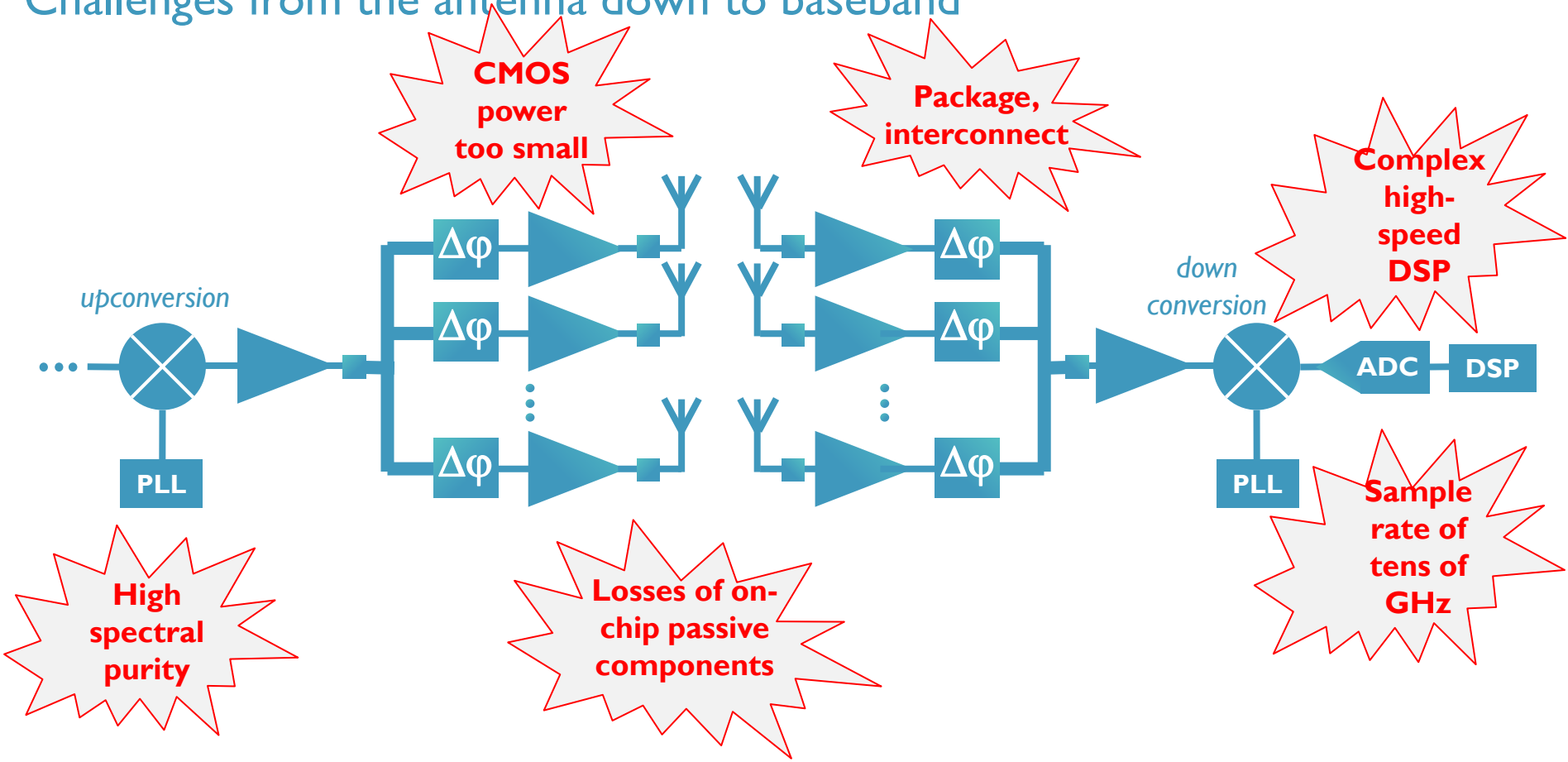
$$C = B\log_2\left(1+\frac{S}{N}\right)$$



- Wide bandwidths available at higher frequencies
  - W-band: >17GHz
  - D-band: > 30GHz
  - 802.15.3d: > 50GHz

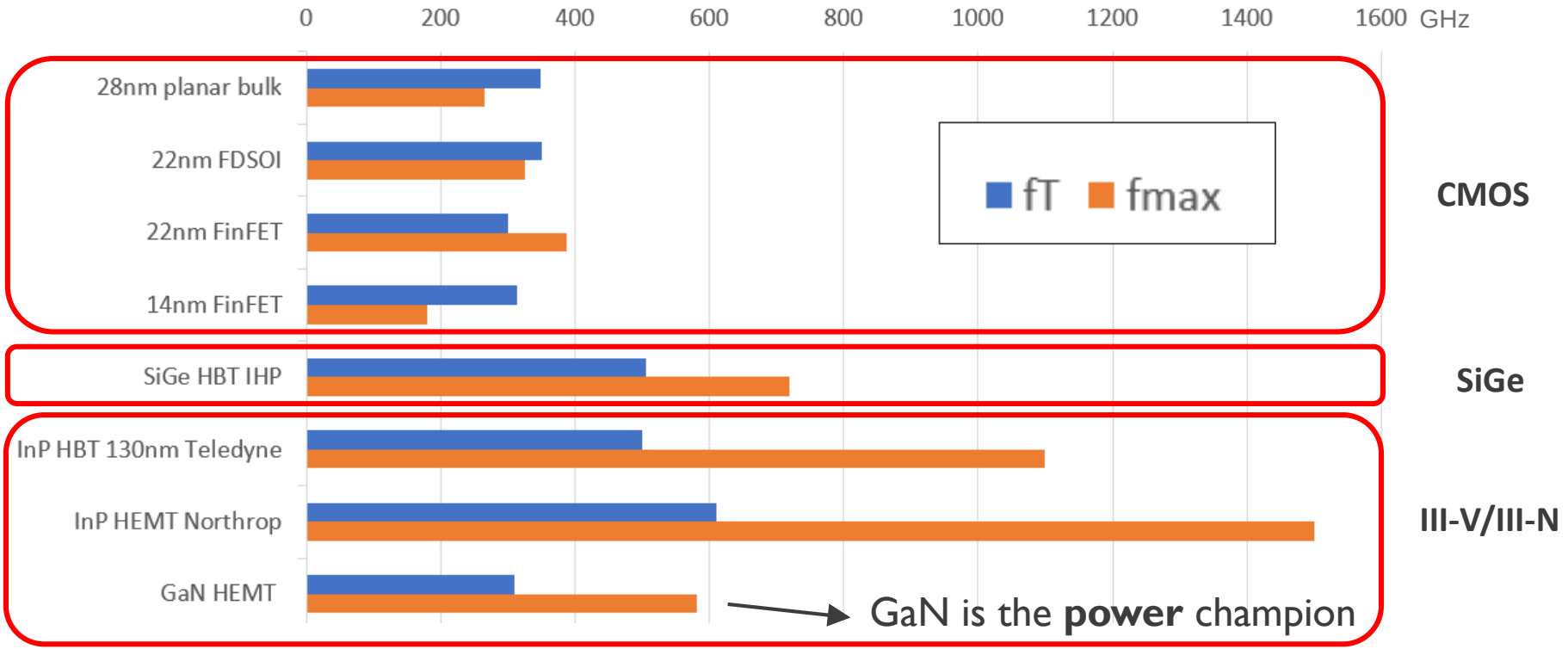


Challenges from the antenna down to baseband



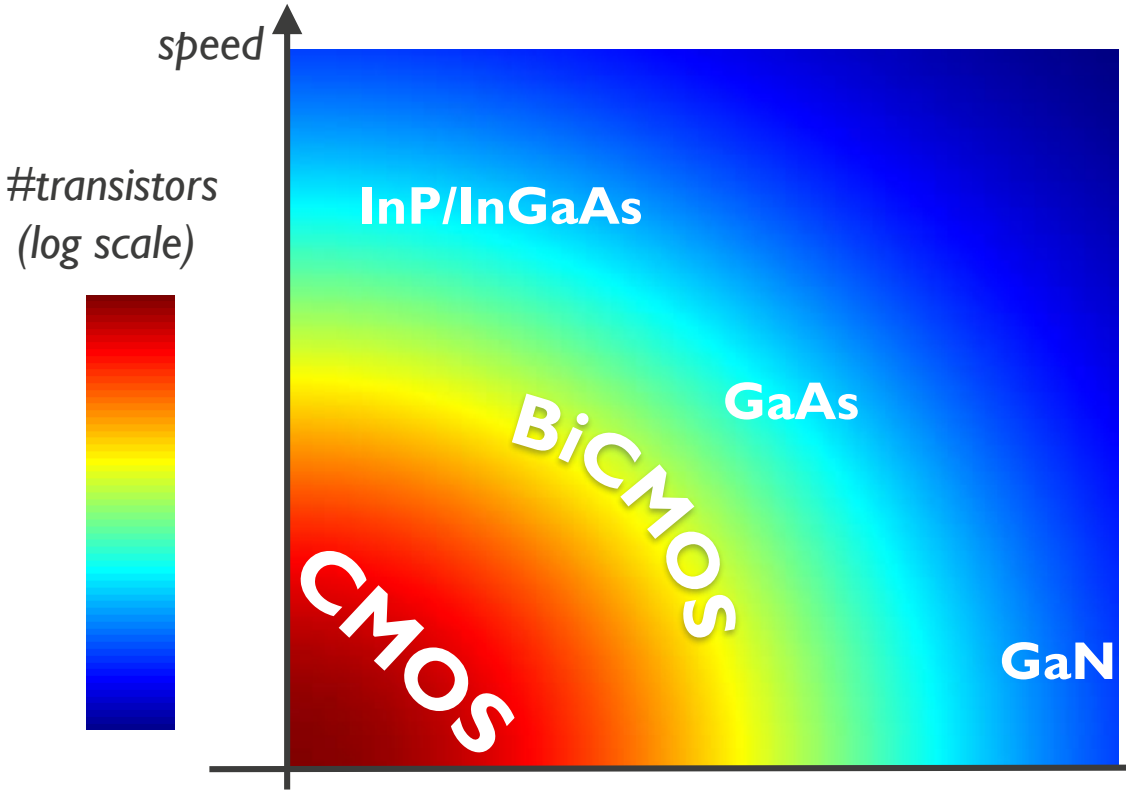
imec

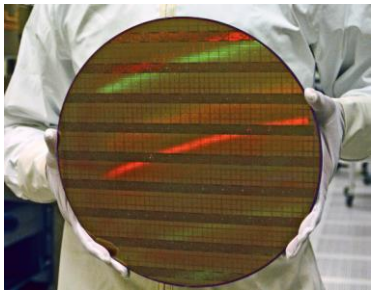
For THz range and high power, CMOS is saturating.
The champions are the III-V/III-N devices`



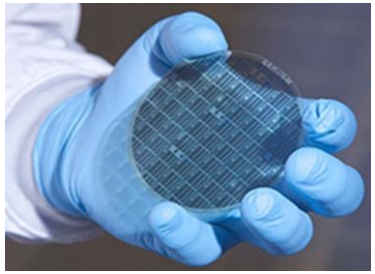
Current landscape in foundry technologies

CMOS beats any other technology in integration level





silicon



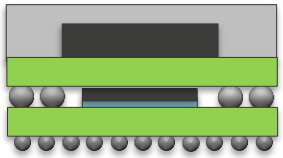
III-V

III-V technologies use very few metals (gold), extrinsic parasitics not optimized

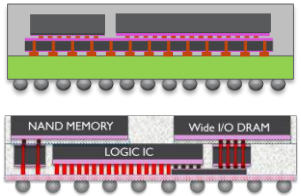
The 3D interconnect technology landscape

3D-SIP

Package stacking

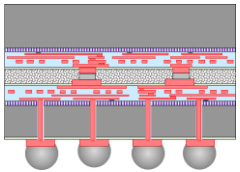


Multi-die Packaging Interposer "2.5D" Embedded Die



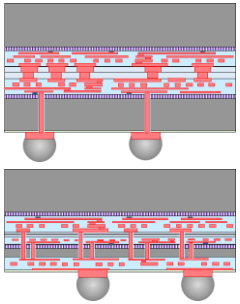
3D-SIC

Die Stacking µbump

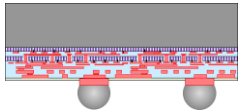


3D-SOC

Wafer-to-Wafer bonding

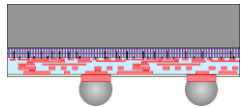


Wafer-to-Wafer Sequential Processing



3D-IC

Transistor Stacking



Interconnect Pitch scaling

1mm 400µm 100 µm 10 µm 1µm 100nm

Interconnect density (#/mm²)

1 10 100 1000 10^4 10^5 10^6 10^7 10^8

imec

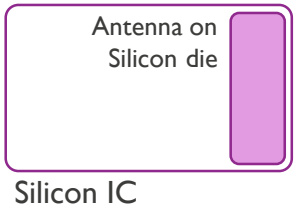
ADC and DSP

- Baseband bandwidths grow to tens of GHz
  - ADCs in the tens of Gsps range are needed
  - Initially low spectral efficiency is required
  - But eventually move to ~64QAM or so → ~7 to 9 bits

- DSP speed must follow
  - Very high speed
  - Heavy parallelization
  - Multi-path is less frequent but can happen
  - Equalizer schemes must be revisited to cope with tens of Gbauds equalization
    - Digital vs analog
    - Pre- vs post equalization to bring complexity where it can be afforded (AP, BS)

Chip-antenna co-design above 100GHz

EM and thermal challenges

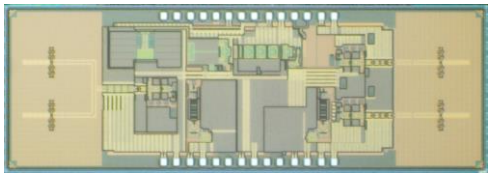


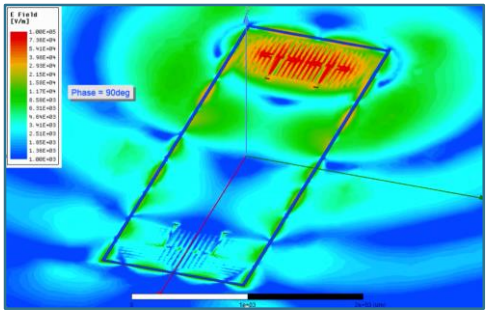
Challenge:
On-chip antenna design in CMOS

Challenge:
On-chip antenna design & low-parasitics IC/IC interconnect

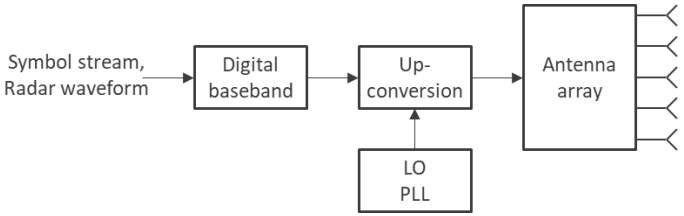
Challenge:
On-interposer antenna design & low-parasitics IC/IC interconnect

140 GHz FMCW radar, 10GHz BW,
with antenna on chip,
in standard 28 nm CMOS
(3 dB gain, 11dBm EIRP, 1 mm^2 area)

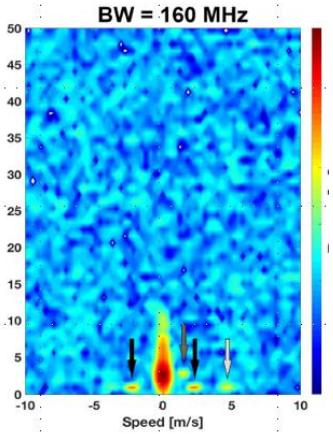




Radar-Communications convergence



- Observation:
  - Radar and communications hardware, DSP and antennas are very similar
  - Radar and communications use more and more multiple antennas/MIMO concepts
  - Mm-wave comm (e.g. WiGig, 11ay at 60GHz) and mm-wave radar (automotive 77/79GHz) are well mastered technologies
  - Some wireless communications functionality have much in common with radar
    - Radar range profile vs channel estimation
    - MIMO radar vs MIMO channel estimation (channel between all possible TX-RX pairs)
  - Some developments and standardization already bridge the gap
    - Wi-Fi based people detection, fall detection
    - Some products, software stack appear (Origin Wireless, Cognitive Systems, Aura, ...)
    - Wi-Fi sensing (IEEE 802.11 SENS TIG/SG)



Radar-Communications convergence

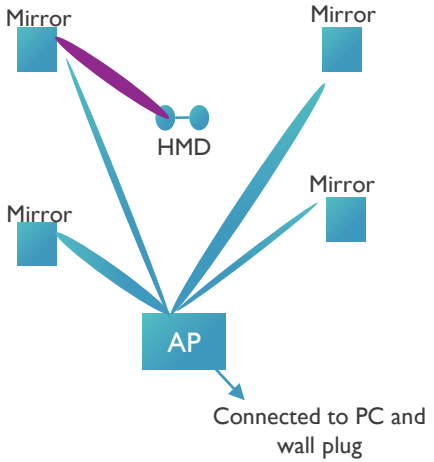
Green field for THz

- But much more is possible
- Massive MIMO/large phased array systems can enable high angle resolution radar for target tracking and environment mapping
- Distributed massive MIMO can be turned into bistatic or multi-view radars
- Mm-wave/THz systems, with multi-GHz bandwidth, can have cm-scale range resolution
- Both functionalities can support each other for
  - Improved performance
  - Yet-to-discover new joint modes of operation

nLOS problem at mm-wave/THz

Robust coverage with Phased Array Mirror

- Using phased array based relays/re-routers to create alternate LOS path while maintaining low latency
  - Angle of incidence ≠ Angle of reflection
- Advantages
  - Overcomes blockage/shadowing
  - No Synchronization, handoff, and latency issues
  - Low cost and lower power alternative
- Challenges
  - Self-interference problem ➔ full duplex design techniques
  - Multi-user



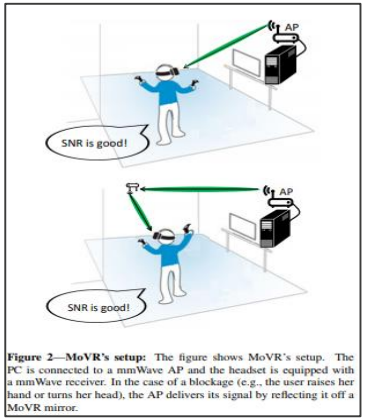


Figure 2—MoVR's setup: The figure shows MoVR's setup. The PC is connected to a mmWave AP and the headset is equipped with a mmWave receiver. In the case of a blockage (e.g., the user raises her hand or turns her head), the AP delivers its signal by reflecting it off a MoVR mirror.

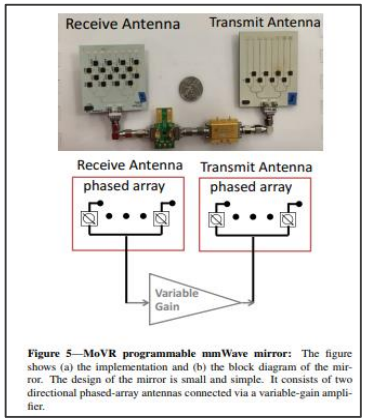


Figure 5—MoVR programmable mmWave mirror: The figure shows (a) the implementation and (b) the block diagram of the mirror. The design of the mirror is small and simple. It consists of two directional phased-array antennas connected via a variable-gain amplifier.

Source: Dina Katabi's MIT

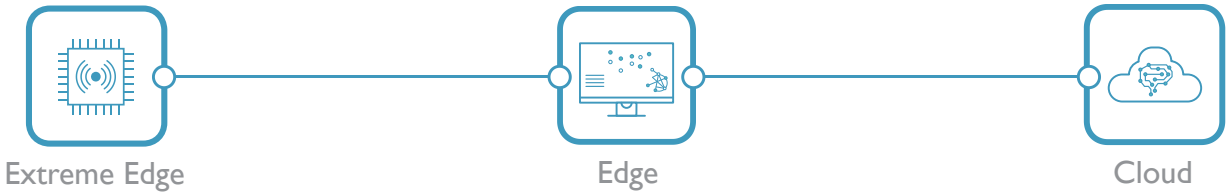
Extreme Edge Processor

Yesterday

Cloud AI with extreme edge data

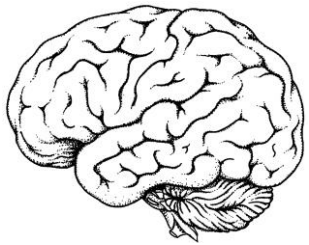
ISSUES:

- **Data growing faster than connectivity**
- **Privacy**
- **Robustness**
- **Latency**
- **Power**



DATA

Decisions



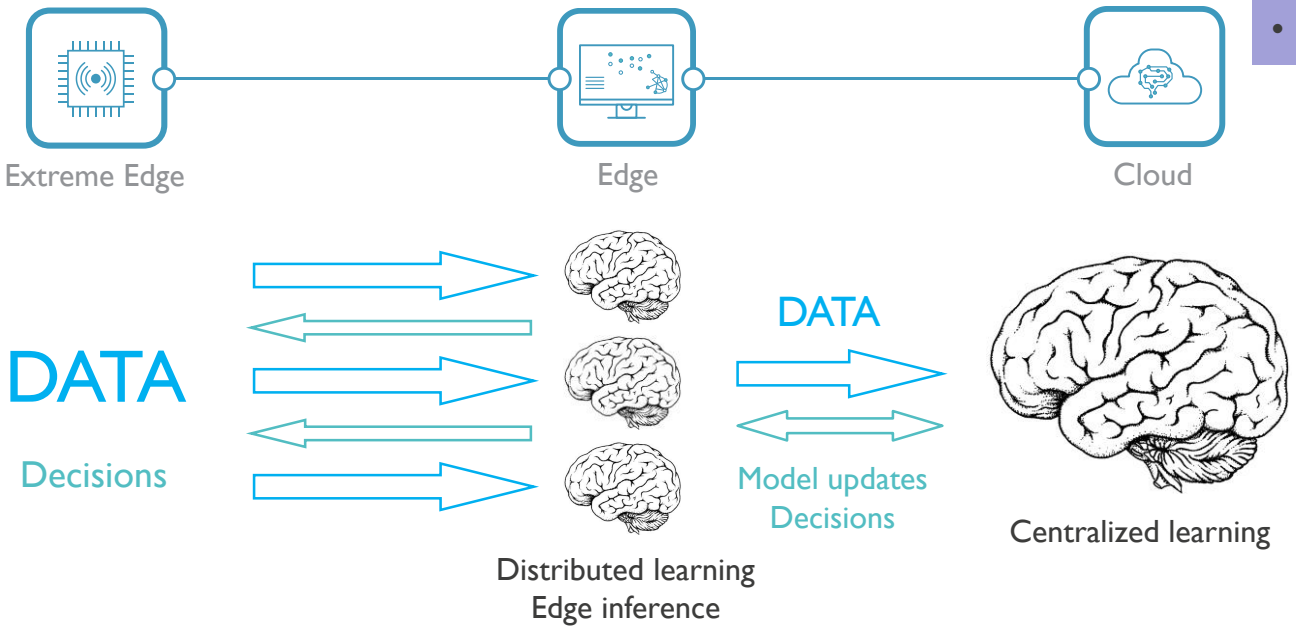
Learning & Inference

Today

Decentralized AI

ISSUES:

- ~~Data growing faster than connectivity~~
- ~~Privacy~~
- Robustness
- Latency
- Power

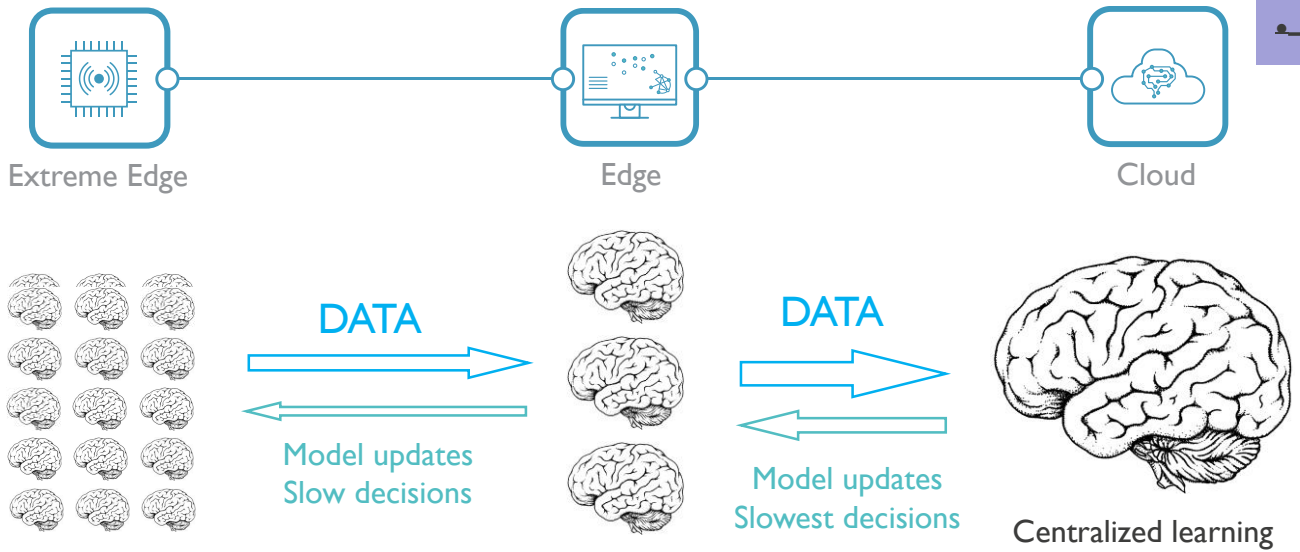


Tomorrow

Moving AI to the extreme edge

ISSUES:

- ~~Data growing faster than connectivity~~
- ~~Privacy~~ even better
- ~~Robustness~~
- ~~Latency~~
- ~~Power~~



Extreme edge AI

(fast, low power, safe, autonomous)

Analog vs digital trade-off

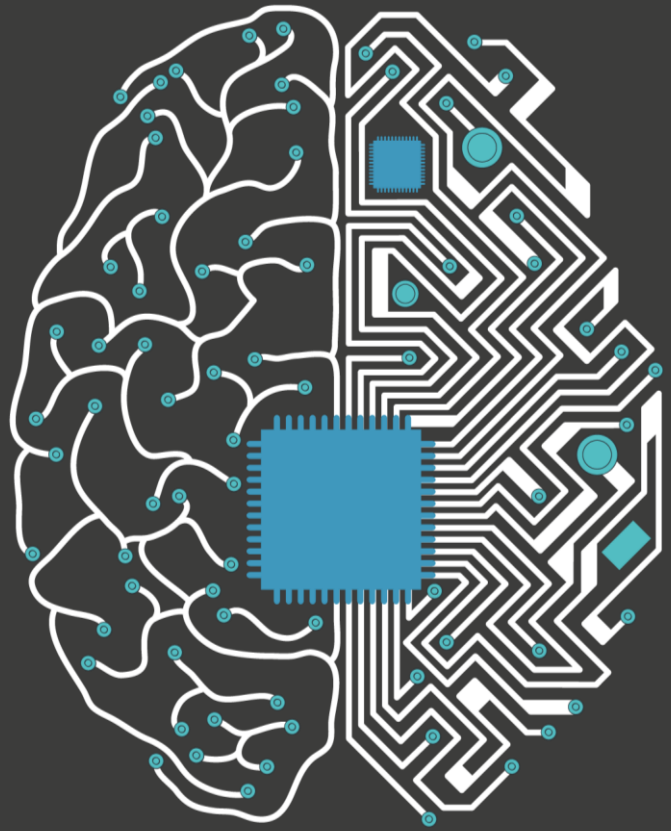
Distributed learning
Edge inference

Neuromorphic Processor

Dimensions along which compute technologies can be neuromorphic

- Sequential vs. massively parallel
- Clocked vs. asynchronous
- Event-based processing
- Spiking NN
- Analog vs. digital
- Von-Neumann vs. non-Von Neumann (compute-in-memory)
- High-bit to Low-bit precision
- Learning from much labeled data vs. learning from little unlabeled data

This is NOT a traditional CPU/GPU/TPU/FPGA/ARM/...



imec

Conclusions

Conclusions

Key research areas

- Communications above 100 GHz at tens of Gbit/s call for:
  - Better devices for the RF part: III/V, III/N or GaN on CMOS
  - Faster ADCs, tens of Gsps, 7+ bits
  - Rethinking equalization schemes
  - Intelligent non-specular mirror might help in some cases
  - Chip-antenna co-design (antennas on chip become feasible)
  - Exploiting the third dimension for bonding/stacking

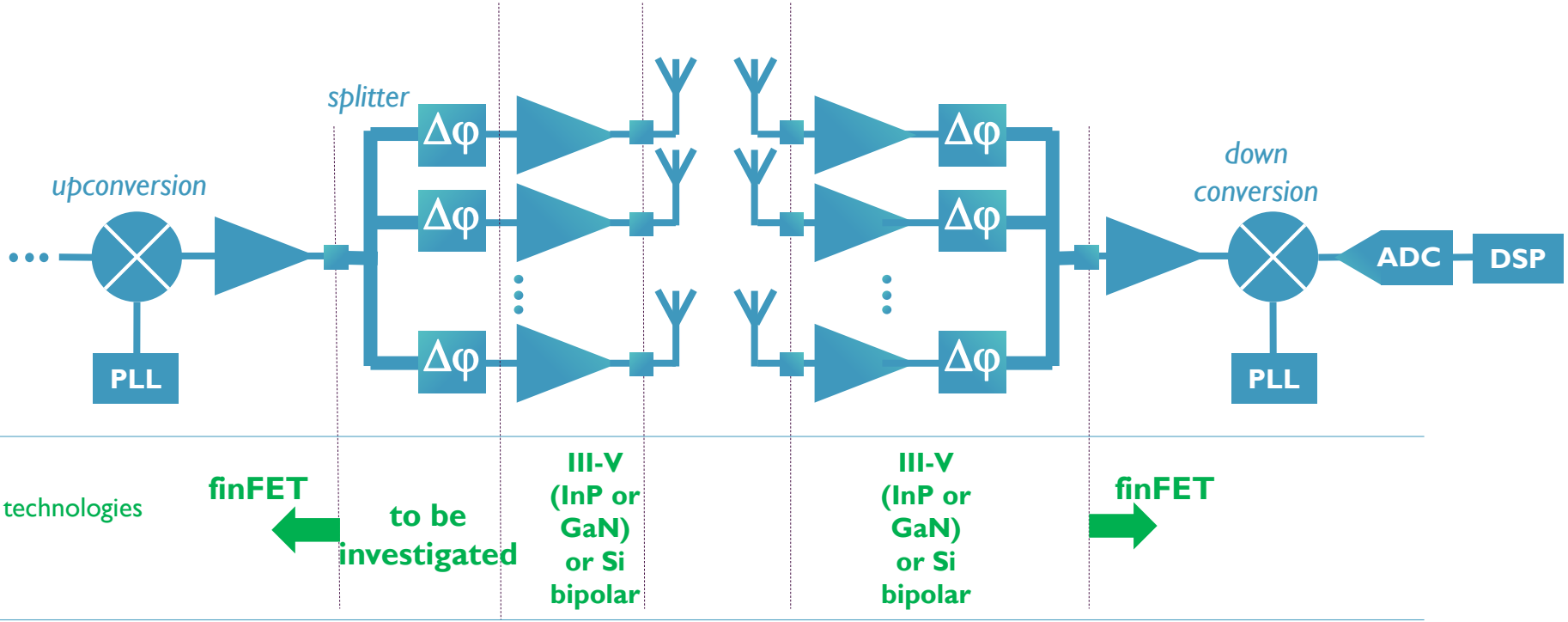
- Joint radar and communications
  - Leveraging massive arrays and mm-wave/THz bandwidth for high througput and high resolution
  - New joint modes of operation

- Extreme edge computing is a new paradigm calling for
  - A new breed of processor
  - New learning modes (mostly unsupervised)
  - Analog vs digital for extreme low power
  - Computing-connectivity tarde-off

embracing a better life

Back-up slides

CMOS cannot do it alone anymore

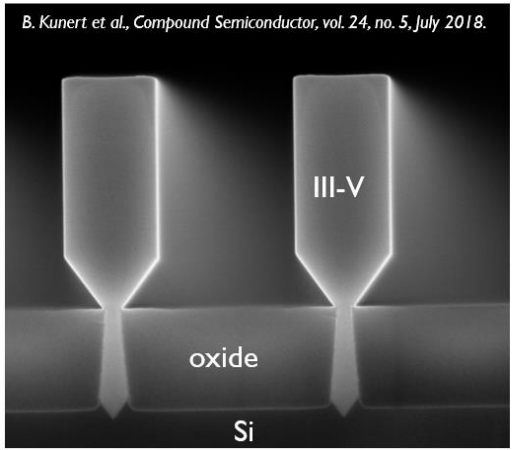


Marrying III-V with silicon?

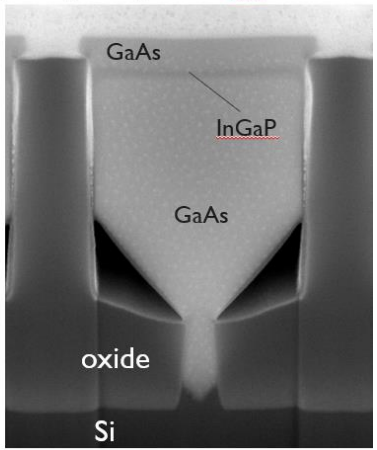
Combine best of both worlds

- Several attempts to improve yield and economics of III-V
  - GaN on 300 mm Si wafers instead of GaN on SiC
- High-mobility III-V combined with CMOS
  - Monolithic, see
  - Challenge: overcome lattice mismatch, mismatch in thermal coefficients

Free-standing nano-ridges

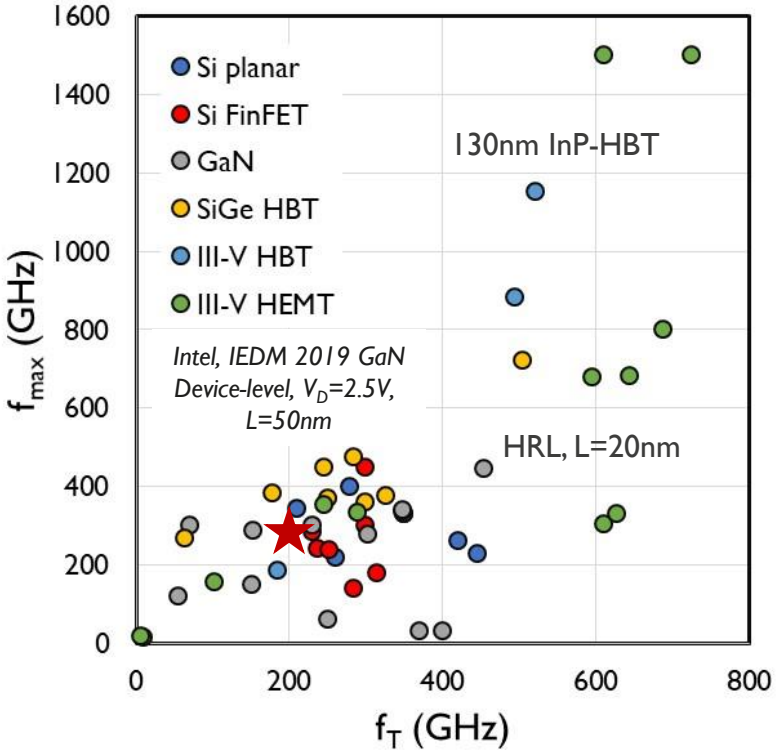


Templated growth: full GaAs npn-HBT stack

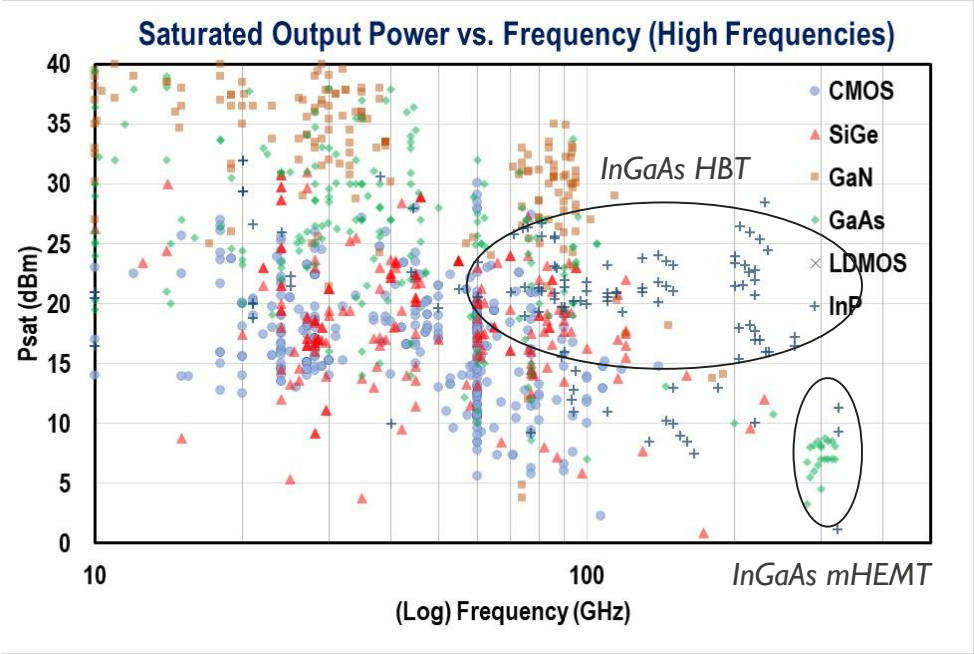


- Alternative: 3D combination of CMOS with III-V
  - Wafer-level hybrid bonding
  - Die-to-wafer, wafer-to-wafer, die-to-die
  - Sequential 3D

Which IC technology for > 100 GHz ?



https://gems.ece.gatech.edu/PA_survey.html



III-V devices outperform Si(Ge) & GaN devices in speed, output power and efficiency > 100GHz

imec